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| **Digital circuits laboratory class** | **Year 2024, exercise 2** |
| Author: Jakub Turkowski | Title of the exercise: Combinational logic circuits |
| Laboratory group number: 2 | Week day: Tuesday  Realization date: 19.03.2024  Hours of the lab: 15:15-16:55 |

F(abcd)=(((a+b)’+c’)’+d)’=d’((a+b)’+c’)’=d’(c’+(a+b)’)=(a’b’d’)+(c’d’)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB  CD | 0 0 | 0 1 | 1 1 | 1 0 |
|  |
| 0 0 | 1 | 1 | 1 | 1 |  |
| 0 1 | 0 | 0 | 0 | 0 |  |
| 1 1 | 0 | 0 | 0 | 0 |  |
| 1 0 | 1 | 0 | 0 | 0 |  |

SoP = c’d’+a’b’d’

Double negate it and we get:

SoP = ((c’d’)’(a’b’d’)’)’

This gives us the circuit using only NAND gates. To get the MUX circuit I took a and b to be S0 and S1 respectively and adjusted the inputs I0 to I4 to take the values of CD for which the function returns true. So I1 to I3 = c’d’ and I0 = d’.

Obraz zawierający tekst, diagram, zrzut ekranu, linia

Opis wygenerowany automatycznie

F(abc)=((abc’)+(a’b’c))’=(a’+b’+c)(a+b+c’)=(a’b)+(a’c’)+(b’a)+(b’c’)+(ca)+(cb)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB  C | 0 0 | 0 1 | 1 1 | 1 0 |
|  |
| 0 | 1 | 1 | 0 | 1 |  |
| 1 | 0 | 1 | 1 | 1 |  |

SoP = a’b+b’a+a’c’+ac

After double negation it becomes:

SoP=((a’b)’(b’a)’(a’c’)’(ac)’)’

This gives us the circuit using only NAND gates. To get the MUX circuit I took c to be S0 and adjusted the inputs I0 to I4 to take the values of CD for which the function returns true. So I1 = a+b and I0 = a’+b’.

Obraz zawierający tekst, diagram, Plan, wykres

Opis wygenerowany automatycznie

Obraz zawierający zrzut ekranu, linia

Opis wygenerowany automatycznie